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10/707,797	01/13/2004	Wayne F. Ellis	BUR920030151US1	1796

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EXAMINER	
MERANT, GUERRIER	
ART UNIT	PAPER NUMBER
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/707,797	ELLIS ET AL.	
	Examiner	Art Unit	
	Guerrier Merant	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Final Rejection

Response to Amendment

1. Applicant's arguments/amendment, filled 08/28/08, with respect to the rejection(s) of claims 7-26, have been fully considered and are entered.

Response to Arguments

2. As per claim 14, the Applicant argued that the prior arts of record fails to teach *"reducing the corresponding row or column weight values of the remaining failed row and column addresses in the third memory element that share defective memory addresses with the repaired rows or columns."* The Examiner respectfully disagrees. **Park et al (US 6,243,307 B1)** teaches decreasing or reducing by 1 the number of failed row/column addresses once the corresponding row/column addresses have been corrected or repaired (e.g. col. 14, lines 35-47- see fig. 11A; col. 14, lines 56-67- fig. 11B).

3. As per claim 21: In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "a third memory element for accumulating ones of the row and column addresses **not already contained in said first and second memory elements**") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Therefore, the Applicant's arguments with regard to the rejection of claim 14 are not persuasive.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> a. The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. Claims 7-13 and 21-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

b. Claim 7 recites the limitation "failed row and column addresses" in line 11. There is insufficient antecedent basis for this limitation in the claim.

c. Claim 21 recites the limitation "to be-repaired row and column addresses" in line 13-14. There is insufficient antecedent basis for this limitation in the claim

d. As per claims 7 and 21: It is not clear to the Examiner when or how the first and second memory elements are being loaded. For instance, the first and second memory elements are empty when they are no errors in the memory circuit. In that case, the third memory element would be the only memory element with address data and the determining steps would not provide accurate results.

e. Claims 8-13 and 22-26 inherit the 35 U.S.C. 112, second paragraph issued of the independent claims 7 and 21 by virtue of their dependency.

Claim Objections

6. Claim 7 is objected to because of the following informalities:

f. As per claim 7, in line 26, "**addressed**" should be changed to **addresses**.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> g. A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 14, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Irrinki et al (US 5,987,632)** and further in view of **Park et al (US 6,243,307 B1).**

9. As per claim 14: **Irrinki et al** substantially a method of providing BIST redundancy allocation to an embedded memory system, comprising the steps of:

identifying failed row and column addresses of defective memory blocks in said embedded memory system *(e.g. col. 3, lines 56-63; col. 4, lines 6-17; col. 5, lines 20-52)*;

transferring said failed row and column addresses associated with the most fails from said third memory element to first *(e.g. items 310, 314, fig. 3)* and second memory elements *(e.g. items 320, 324, fig. 3)* according to a decision algorithm and repairing or

correcting said failed row addresses in the first memory element by assignment of redundant rows and repairing the failed column addresses in the second memory element by assignment of redundant columns *(e.g. col. 6, lines 35-65)*.

But **Irrinki et al** fails to teaches a third memory element for accumulating the failed row and column addresses transmitted from said BIST and assigning them a particular weight value based on the number of like addresses already accumulated in said third memory element and their relative locations within the memory system; and reducing the corresponding row or column weight values of the remaining failed row and column addresses in the third memory element that share defective memory addresses with the repaired rows or columns. However, **Park et al (US 6,574,757 B1)**. **Park et al** teaches an integrated redundancy architecture for providing BIST redundancy allocation to an embedded memory system, the architecture comprising:

a BIST *(e.g. item 11, fig. 1)* for identifying and transmitting row and column addresses from failed embedded memory *(e.g. col. 6, lines 49-65);*

a memory element (e.g. fig. 6A-6J) for accumulating the failed row and column addresses transmitted from said BIST and assigning each of the failed row and column addresses a particular weight value (e.g. *count the number of failed row or column addresses that matches the failed column or row that are already stored*) based on the number of like addresses already accumulated in said third memory element and their relative locations within the memory system (e.g. col. 10, lines 6-46);

and means for allocating assigning ones of the failed row and column addresses having weights (or number of defective cells) greater than a threshold for permanent storage in said first or second memory element (e.g. col. 11, lines 39-64).

And reducing the corresponding row or column weight values of the remaining failed row and column addresses in the third memory element that share defective memory addresses with the repaired rows or columns (e.g. col. 14, lines 35-47- see fig. 11A; col. 14, lines 56-67- fig. 11B).

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to implement the teaching of **Irrinki et al** with the one taught by **Park et al** in order to "*maintain almost constant repair coverage, although the number of the redundancies and the number of the faults are increased" (e.g. col. 15, lines 60-65- Park et al).*

10. Claim 18: **Irrinki et al** and **Park et al** teach an integrated redundancy method as in claim 14 above, wherein said third memory element includes a register *(e.g. item 300, fig. 1)* for accumulating the failed row and column addresses transmitted from said BIST *(e.g. see figs. 6;* **Park et al***).*

11. Claims 19-20: **Irrinki et al** and **Park et al** teach an integrated redundancy method as in claims 7, 14 & 21 above, further comprising a finite state machine *(e.g. item 210, fig. 2;* **Irrinki et al**) having a decision algorithm, said finite state machine in

electrical communication with said first memory element, said second memory element, and said third memory element *(e.g. col. 4, lines 55-67 & col. 5, lines 28-51;* **Irrinki et al**).

12. Claim 16: **Irrinki et al** and **Park et al** teach a method as in claim 14 above, wherein said first memory element includes a register for storing said failed row addresses *(e.g. item 312, fig. 3;* **Irrinki et al**).

13. Claim 17: **Irrinki et al** and **Park et al** teach an integrated circuit and method as in claims 14 and 21 above, wherein said second memory element includes a register for storing said failed column addresses (e.g. item 322, fig. 3; **Irrinki et al**).

14. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Irrinki et al** and **Park et al** as applied to claims 7, 14 and 21 above, and further in view of **Ohtani et al (US 2002/0196683 A1)**.

15. As per claim 15: **Irrinki et al** and **Park et al** fail to teach said first, second, and third memory elements include the function of content addressable memory. However, **Ohtani et al** teaches a circuit/method for of providing BIST redundancy allocation to an embedded memory system comprising storage elements (e.g. items MCR11, MCR12,

MCC11 fig. 3) and wherein the storage elements include the function of content addressable memory *(e.g. [0175], [0178], and [0187]).*

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to replace the memory of **Irrinki et al** and **Park et al** with the memory of **Ohtani et al** in order to accomplish the same function.

Allowable Subject Matter

16. Claims 7-13 and 21-26 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

17. The following is an examiner's statement of reasons for allowance: The prior arts of record fail to teach a third memory element for accumulating ones of the row and column addresses not already contained in said first and second memory elements.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Exr. Merant Guerrier whose telephone number is (571) 270-1066. The examiner can normally be reached Monday through Thursday from 10: 30 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis Jacques, can be reached on (571) 272-6962. Draft or Informal faxes, which will not be entered in the application, may be submitted directly to the examiner at (571) 270-2066.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Guerrier Merant
10/27/08

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